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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/605,326

09/23/2003

Fang-Yu Yeh

11209-US-PA

2325

31561

7590

08/24/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER

SMOOT, STEPHEN W

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,326	YEH ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 September 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office action is in response to application papers filed on 23 September 2003.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character not mentioned in the description:
202a in Figs. 2F, 2G.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method of Forming a Semiconductor Device with a Non-Conformal Liner Layer that is Thinner on Sidewall Surfaces.

3. The disclosure is objected to because of the following informalities:

In paragraph [0028], line 5, change "show" to --shown-- to correct grammar;

In paragraph [0028], line 6, change both appearances of "show" to --shown-- to correct grammar; and

In paragraph [0028], line 7, change "show" to --shown-- to correct grammar.

Appropriate correction is required.

Claim Objections

4. Claims 2-5, 9, 11-15 are objected to because of the following informalities:

In claim 2, line 7, change "has" to --have-- to correct grammar;

In claim 3, line 2, change "comprises" to --comprise-- to correct grammar;

In claim 4, line 5, change "has" to --have-- to correct grammar;

In claim 5, line 3, change "comprises" to --comprise-- to correct grammar;

In claim 9, line 2, change "sidewall" to --sidewalls-- to correct grammar;

In claim 9, line 5, change "sidewall" to --sidewalls-- to correct grammar;

In claim 11, line 8, change "conductive" to --gate-- for proper antecedence to lines 3-4;

In claim 11, line 10, change "conductive" to --gate-- for proper antecedence to lines 3-4;

In claim 12, line 5, change "has" to --have-- to correct grammar;

In claim 13, line 2, change "comprises" to --comprise-- to correct grammar;

In claim 14, line 5, change "has" to --have-- to correct grammar; and

In claim 15, line 3, change "comprises" to --comprise-- to correct grammar.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the sidewalls" in line 7;

Claim 1 recites the limitation "the exposed substrate" in line 8;

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Claim 1 recites the limitation "the liner layer on the substrate surface" in line 10;

Claim 2 recites the limitation "the cap layers" in line 6;

Claim 2 recites the limitation "the growth of the oxide film" in lines 7-8;

Claim 4 recites the limitation "the growth of the oxide film" in line 6;

Claim 6 recites the limitation "the step of forming the conductive structures" in lines 1-2;

Claim 7 recites the limitation "the sidewall metal silicide layer" in line 4;

Claim 8 recites the limitation "the sidewall metal silicide layer" in line 4;

Claim 11 recites the limitation "the sidewalls" in line 8;

Claim 11 recites the limitation "the exposed substrate" in line 9;

Claim 11 recites the limitation "the liner layer on the substrate surface" in line 11;

Claim 12 recites the limitation "the growth of the oxide film" in line 6;

Claim 13 recites the limitation "the ions implanted into the sidewalls" in lines 2-3;

Claim 14 recites the limitation "the growth of the oxide film" in lines 5-6;

Claim 17 recites the limitation "the sidewall metal silicide layer" in line 4; and

Claim 18 recites the limitation "the sidewall metal silicide layer" in line 4.

There is insufficient antecedent basis for these limitations in claims 1-2, 4, 6-8, 11-14, 17-18. The examiner notes that claim 13 would have proper antecedence for "the ions implanted into the sidewalls" if its claim dependency was changed to depend on claim 12.

Claims 2-10 are rejected under 35 U.S.C. 112, second paragraph, because they depend on claim 1; and

Claims 12-19 are rejected under 35 U.S.C. 112, second paragraph, because they depend on claim 11.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-2, 6-7, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang (US 6,268,272 B1) in view of Chang et al. (US 5,817,562).

Referring to Figs. 4A-4C and column 4, lines 23-56, Jang (US 6,268,272 B1) discloses a method of forming a polycide gate electrode with the following features:

- A gate stack comprising gate oxide layer (41), polysilicon layer (42), titanium disilicide layer (43), and mask oxide layer (44) formed on a silicon substrate (40) that is patterned into a gate electrode by selective etching;
- The mask oxide layer (i.e. a cap layer) can alternatively be a mask nitride layer (also see column 3, line 67 to column 4, line 3);
- Silicon ions (Si) are implanted into the sidewalls of the gate electrode as shown in Fig. 4B;

- The gate electrode is then re-oxidized to form oxide (45) on the sidewalls of the gate and on the substrate (40) surface as shown in Fig. 4C; and
- As shown in Fig. 4C, the oxide (45) on the substrate (40) is thicker than the oxide (45) on the sidewalls.

These are limitations set forth in claims 1-2, 6-7, 9 of the applicant's invention.

However, Jang (US 6,268,272 B1) lacks plural conductive structures (a limitation of claim 1), an insulation layer covering the conductive structures (a limitation of claim 1), the step of patterning the insulation layer to form a contact opening between two conductive structures (a limitation of claim 1), and forming a spacer on sidewalls of the conductive structures (a limitation of claim 9).

Referring to Figs. 4-6 and column 6, line 17 to column 7, line 6, Chang et al. teach a gate electrode structure that includes plural gate electrodes (3), sidewall spacers (26, 28), an insulating layer (32) covering the gate electrodes (3), and source/drain contact opening (9) formed between neighboring gate electrodes.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Jang (US 6,268,272 B1) and Chang et al. in order to form source/drain contact openings, as taught by Chang et al., that correspond to the polycide gate electrodes of Jang (US 6,268,272 B1).

Chang et al. recognize that a plurality of gate electrodes are used in the Ultra Large Scale Integration of field effect transistors (see column 1, lines 21-29). Insulating interlayers are known in the art as a way to isolate gate electrodes from overlying metallization layers, contact openings are known in the art as a way to make electrical

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connections to field effect transistors, and sidewall spacers are known in the art as a way to isolate contact openings to source/drain regions from gate electrodes.

9. Claims 11-12, 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang (US 6,268,272 B1).

Referring to Figs. 4A-4C and column 4, lines 23-56, Jang (US 6,268,272 B1) discloses a method of forming a polycide gate electrode with the following features:

- A gate stack comprising gate oxide layer (41), polysilicon layer (42), titanium disilicide layer (43), and mask oxide layer (44) formed on a silicon substrate (40) that is patterned into a gate electrode by selective etching;
- The mask oxide layer (i.e. a cap layer) can alternatively be a mask nitride layer (also see column 3, line 67 to column 4, line 3);
- Silicon ions (Si) are implanted into the sidewalls of the gate electrode as shown in Fig. 4B;
- The gate electrode is then re-oxidized to form oxide (45) on the sidewalls of the gate and on the substrate (40) surface as shown in Fig. 4C; and
- As shown in Fig. 4C, the oxide (45) on the substrate (40) is thicker than the oxide (45) on the sidewalls.

These are limitations set forth in claims 11-12, 16-17 of the applicant's invention.

However, Jang (US 6,268,272 B1) does not teach or suggest a plurality of gate electrodes, which is a limitation of claim 11.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply Jang's method to plural gate electrodes since it has been held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced [see *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960)].

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jang et al. (US 6,255,206 B1) teach thermal oxidation of a polycide gate electrode. Koga teaches rapid thermal nitridation and rapid thermal oxidation of side surfaces of a polycide gate electrode.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SWS

Stephen W. Smoot
Patent Examiner
Art Unit 2813